Sensitivity Characterization of a COTS 90-nm SRAM at Ultra Low Bias Voltage

Juan Antonio Clemente, Guillaume Hubert, Francisco J. Franco, Francesca Villa, Maud Baylac, Hortensia Mecha, Helmut Puchner and Raoul Velazco

***Abstract*—This paper presents the characterization of the sensitivity to 14-MeV neutrons of a Commercial Off-The-Shelf (COTS) 90-nm Static Random Access Memories (SRAMs) manufactured by Cypress Semiconductor, when biased at ultra low voltage. Firstly, experiments exposing this memory at 14-MeV neutrons, when powering it up at bias voltages ranging from 0.5V to 3.3V, are presented and discussed. These results are in good concordance with theoretical predictions issued by the modeling tool MUSCA-SEP^3 (*MUlti-SCAles Single Event Phenomena Predictive Platform*). Then, this tool has been used to obtain Soft Error Rate (SER) predictions at different altitudes above the Earth's surface of this device vs. its bias voltage. Finally, the effect of contamination by α particles has also been estimated at said range of bias voltages.**

***Index Terms*—COTS, SRAM, neutron tests, radiation hardness, reliability, soft error, low-bias voltage**

I. Introduction

COmmercial CMOS SRAMs have recently drawn the attention of researchers and manufacturers of complex electronic systems in fields such as avionics and aerospace. The reason is their affordable cost and that many modern devices implement error detection and protection mechanisms, such as the well-known Error Correcting Codes (ECCs) [1], [2], which make them very reliable to the so-called Single Event Effects (SEEs) [3].

Hence, these SRAMs can potentially be used in environments where energy efficiency is a real concern [4]. It has been reported that modern SRAMs can keep the information even if the bias voltage falls down to 15-20% of the nominal value, which can be used to effectively reduce the power dissipation [5]. However, as the bias voltage decreases, the critical charge to trigger a SEE decreases as well [6], [7]. Thus, bitflips are much more likely to occur when the circuit operates at ultra-low bias voltage, not far above from the minimum power supply that allows retention of data. This fact is valid for Single Event Upsets (SEUs) -in particular for Single Bit Upsets (SBUs), and for Multiple Cell Upsets (MCUs)- and even for Multiple Bit Upsets (MBUs) with the possible exception of the Single Event Latch-ups (SELs). Even electrons, which constitute the lightest charged particles, can provoke bitflips in 45-nm CMOS SRAMs at ultra-low bias voltage [5].

Previous studies have pointed out the relationship between the bias voltage reduction and the sensitivity against SEEs in different technologies of SRAMs [8], [9]. In [10], the authors studied the sensitivity against 15-MeV neutrons of a COTS Advanced Low Power SRAMs (A-LPSRAM), manufactured in 150-nm CMOS technology, at 0.5V - 3.3V. However, to the authors' knowledge, little work has been carried out on COTS SRAMs at ultra-low bias voltages under natural radiation: cosmic rays or α emitter impurities.

This paper presents the characterization of the sensitivity of a CMOS SRAM manufactured by Cypress Semiconductor with 90-nm technology, when powered up at voltages ranging from 0.5V to 3.3V. Radiation ground tests were performed with 14-MeV neutrons at the GENEPI2 neutron source (*GEnerator of NEutrons Pulsed and Intense*) [11], [12]. These results were in concordance with theoretical neutron cross-section predictions issued by the MUSCA-SEP^3 modeling approach, developed at the French Aerospace Lab (ONERA), in Toulouse, France [13]. SER predictions at different bias voltages for a spectra including protons, neutrons and muons, as well as for α-particles contamination have been also performed with MUSCA-SEP^3 and discussed in the paper.

The performed tests issued up to several thousands of bitflips per round, especially for the lowest power supplies. Very interesting conclusions could be drawn, including a clear trend in the SBU/MCU sensitivity increase at lower bias voltages. The main contributions of this paper with respect to the previous conference version presented at RADECS (*RADiation Effects on Components & Systems*) [14] are:

- The utilization of the proprietary unscrambling information of Cypress to accurately discern SBUs/MCUs instead of the probabilistic methodology presented in [15].
- Novel SER predictions obtained with MUSCA-SEP^3 at different low-bias voltages for different environments: ground, avionics and space.
- A significant extension of the results regarding the SER predictions for the protons, neutrons and muons spectra, and for the α-particles contamination.

This work was supported in part by the Spanish MCINN project TIN2013-40968-P and by the mobility grant "José Castillejo" for professors and researchers.

J. A. Clemente and H. Mecha are with the Computer Architecture Department, Facultad de Informática, Universidad Complutense de Madrid (UCM), Spain, e-mails: ja.clemente@fdi.ucm.es, horten@ucm.es.

G. Hubert is with the ONERA French Aerospace Laboratory, Toulouse, France, e-mail: guillaume.hubert@onera.fr.

F. J. Franco is with the Departamento de Física Aplicada III, Facultad de Ciencias Físicas, Universidad Complutense de Madrid (UCM), Spain, e-mail: fjfranco@fis.ucm.es.

F. Villa and M. Baylac are with Laboratoire de Physique Subatomique et de Cosmologie LPSC, Université Grenoble-Alpes & CNRS/IN2P3, Grenoble, France, e-mails: francesca.villa@lpsc.in2p3.fr, baylac@lpsc.in2p3.fr.

H. Puchner is with Cypress Semiconductor, Technology R&D, 3901 San Jose, CA, USA. e-mail: hrp@cypress.com.

R. Velazco is with the Université Grenoble-Alpes & CNRS, TIMA, Grenoble (France), e-mail: raoul.velazco@imag.fr.

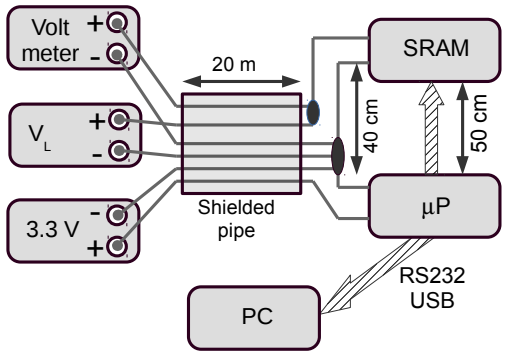

Figure 1. Schematic of connections and length of the cables. A 100-μF capacitor was placed between the power supply and ground in the microcontroller board, and a smaller one (100 nF) in the SRAM board. The cable shield was connected to the ground output of the 3.3 V power supply.

II. Experimental Setup

Tests were carried out on one sample of the CY62167EV30LL-45ZXI CMOS SRAM manufactured by Cypress, which has a capacity of 16 Mbits. It was configured as 2M×8 bits. Due to a bug in the software that performed the read/write operations on the SRAM, the most significant bit of the address port was permanently set to '0' and hence, only half of the memory was examined. However, according to the manufacturer, this memory comprises two 8-Mbit independent blocks, so only one of them was examined. In any case, the number of events that were observed in the memory were significant enough to extract statistical conclusions. The nominal bias voltage of this memory ranges from 2.7V to 3.6V. However, we verified that even with a bias voltage of 0.45V, it retained information.

Static tests were carried out: the memory was initially written with the *checkerboard* pattern (0×55), then it was radiated in rounds of 5 minutes each, and examined after irradiation. Tests were performed at the GENEPI2 facility, which is located at the LPSC (Laboratoire de Physique Subatomique et Cosmologie) in Grenoble, France [11]. Neutrons were produced with an average energy of 14.2 MeV. The target memory was placed 39 mm away from the neutron source.

The test system comprised a motherboard with a PIC18F85J90 microcontroller, which run the test software. This device worked with a 20-MHz quartz clock and, experimentally, we observed that it could operate correctly even with a bias voltage of 1.9V. An extension board with the SRAM under test was attached to it. Both the microcontroller and the SRAM were biased by two independent power supplies, which made possible to tune that of the SRAM from 0V to 3.3V (Figure 1).

The SRAM bias voltage was measured with a Keithley 2001 multimeter directly at the memory board. The three grounds (two for the power supplies, and one for the multimeter) were connected near the extension board for an accurate measurement. That means that six shielded cables, with a length of 20-m each, were necessary to build the test system.

In order to effectively tune the voltage of the SRAM to levels below 2.7V, it was necessary to manually set the address and data buses, as well as the enable signals of the SRAM, to ground. This prevented the activation of the over-voltage protection structures present in this SRAM, which otherwise kept its bias voltage to levels above 2.7V. Therefore, in each experiment, a 0×00 word was always written in the first address in the memory, 0×00000, whichever the pattern was. In any case, let us bear in mind that only 1 byte was sacrificed in a memory with 8 Mbits and, also, this allowed testing and debugging the test software.

Table I
Performed rounds of irradiation (Table I in [14])

Round	V_{CC} (V)	Fluence (n/cm^2)	Number of affected addresses
A	0.50	2.14×10^9	1925
B	0.60	2.14×10^9	1605
C	0.70	2.14×10^9	1469
D	0.80	2.14×10^9	1328
E	0.90	2.14×10^9	1131
F	1.00	2.14×10^9	962
G	1.20	2.14×10^9	782
H [a]	3.30	1.08×10^8	120

[a] Note that Round H was performed at a significantly different flux

III. Experimental Results with 14-MeV Neutrons

Table I shows the successive tests that were performed. The initial voltage supply was 0.5V and the last one, 1.2V. At 1.4V, the memory was no longer functional. These tests were included in a larger campaign of experiments. Thus, due to logistic reasons, we could not perform more experiments at voltages above 1.2V.

A. Sensitivity vs. Bias Voltage

Results at nominal voltage (3.3V, Round H), which were carried out in previous tests in 2013 for a sample of the same batch [15], have also been included in Table I as reference. In that occasion, SRAMs were set at a fairly large distance from the target (40 cm), to limit the neutron flux to approximately 3×10^4 $n{\cdot}cm^{-2}{\cdot}s^{-1}$. Under those conditions, the memories were exposed to a fluence of $1.08{\times}10^8$ $n{\cdot}cm^{-2}$ within 1 hour. It must be taken into account that, after that test, the facility was upgraded so the flux neutron value used in the low-power tests presented in this paper was significantly higher ($4.5{\times}10^7$ $n \cdot cm^{-2} \cdot s^{-1}$).

In rows A-H of Table I, one can roughly observe that, under identical conditions, the number of observed events increases as the power supply decreases. However, those data "as is" cannot be used to estimate the sensitivity of the device because MCUs need to be extracted from the bulk set of errors. In order to discern SBUs/MCUs from the bulk set of errors, proprietary unscrambling information from Cypress was used, which allowed relating addresses involved in the same multiple event. Affected addresses located at a Manhattan distance lower than 5 were grouped in the same MCU. This threshold distance was chosen to detect cells placed in opposite coins of a 3x3 square. Table II shows the MCUs that were detected,

Table II
EVENTS CLASSIFICATION (NORMAL INCIDENCE)

Bias voltage (V)	SBU	2-bit	3-bit	4-bit	5-bit
0.50	1645	96	12	8	2
0.60	1385	89	10	3	0
0.70	1215	96	13	3	1
0.80	1065	97	15	4	0
0.90	876	99	12	4	0
1.00	734	79	16	5	0
1.20	623	69	7	0	0
3.30	86	12	2	1	0
Bias voltage (V)	6-bit	7-bit	8-bit	9-bit	10-bit
0.50	0	0	0	0	1
0.60	0	0	0	0	0
0.70	1	0	0	0	0
0.80	0	0	0	0	0
0.90	0	0	0	0	0
1.00	1	1	0	0	0
1.20	0	0	0	0	0
3.30	0	0	0	0	0

Table III
EXPERIMENTAL CROSS SECTIONS (NORMAL INCIDENCE), IN cm^2/bit

Bias voltage (V)	SBU	2-bit	3-bit
0.50	$8.73 - 9.62$	$4.33 - 6.53$	$3.45 - 11.70$
0.60	$7.31 - 8.13$	$3.98 - 6.10$	$2.67 - 10.20$
0.70	$6.39 - 7.16$	$4.33 - 6.53$	$3.86 - 12.40$
0.80	$5.58 - 6.30$	$4.38 - 6.59$	$4.68 - 13.80$
0.90	$4.56 - 5.21$	$4.48 - 6.71$	$3.45 - 11.70$
1.00	$3.80 - 4.40$	$3.48 - 5.48$	$5.09 - 14.50$
1.20	$3.20 - 3.75$	$2.99 - 4.86$	$1.57 - 8.03$
3.30	$3.79 - 5.86$	$3.42 - 11.60$	$1.34 - 40.00$
	$\times 10^{-14}$	$\times 10^{-15}$	$\times 10^{-16}$
Bias voltage (V)	4-bit	5-bit	6-bit
0.50	$1.92 - 8.78$	$0.14 - 4.02$	$0 - 2.05$
0.60	$0.35 - 4.88$	$0 - 2.05$	$0 - 2.05$
0.70	$0.35 - 4.88$	$0.01 - 3.10$	$0.01 - 3.10$
0.80	$0.61 - 5.71$	$0 - 2.05$	$0 - 2.05$
0.90	$0.61 - 5.71$	$0 - 2.05$	$0 - 2.05$
1.00	$0.90 - 6.50$	$0 - 2.05$	$0.01 - 3.10$
1.20	$0 - 2.05$	$0 - 2.05$	$0 - 2.05$
3.30	$0.14 - 30.80$	$0 - 20.40$	$0 - 20.40$
	$\times 10^{-16}$	$\times 10^{-16}$	$\times 10^{-16}$

and classifies them by their multiplicity. The largest event that was observed was a 10-bit MCU, which occurred at 0.5V.

Finally, Figure 2 shows the cross section of this device for SBUs to 4-bit MCUs, and for different voltage levels. This graph also includes error bars for the experimental cross-section calculations, which have been calculated with 95%-confidence intervals, as explained in [16]. Those of 5-bit to 10-bit MCU cross sections were so wide that it was impractical to include them in the figure. In any case, all the values have also been tabulated in Table III. In this case, it is easy to hint

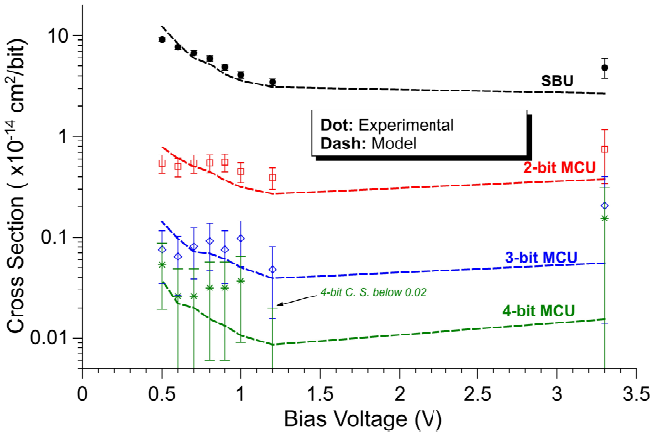

Figure 2. Cross sections of the 90-nm memory studied, for different voltage levels. Dots indicate experimental measurements, whereas the dashed line indicates the predictions issued from MUSCA-SEP3.

the cross sections for 7-bit to 10-bit MCUs, given the very few number of such events that were observed (not included in Table III for the sake of clarity).

Figure 2 also includes predictions issued from the modeling approach MUSCA-SEP^3. The calculations of this tool consider a dynamic neutron spectrum issued from a spectrometer and a technological model (i.e. elementary cell topology), determined through a technical analysis and technological parameters, based on the International Technology Roadmap for Semiconductors (ITRS) [17].

B. Discussion

From the obtained experimental results, it can be easily deduced that the device sensitivity increases as the bias voltage decreases. This sensitivity seems to decrease significantly for the range 0.5V-1V, but for higher voltage values, it clearly flattens (see Figure 2).

As Figure 2 shows, the predictions for SBUs are in very good concordance with the experimental results. However, there are some problems with the interpretation of MCUs. Apparently, there is a soft increase as the power supply approaches 0.5V followed by saturation. This saturation is not predicted by MUSCA-SEP^3. This discrepancy can be attributed to two factors: First, the lack of specific information about the physical layout of the SRAM under test. Second, MUSCA-SEP^3 is a Monte-Carlo tool exposed to randomness in such a way that unusual events occur few times, so the uncertainty in the calculation of unusual events is not negligible.

In any case, the predictions match fairly well the experimental results, with the possible exception of the SBU one at 3.3V. We believe that the reason of such small disagreement is that the experiment with 3.3V (Round H in Table I) was carried out at completely different environmental conditions: On the one hand, the neutron fluence was not the same as in Rounds A-G (let us remember that this experiment was made in 2013), and the uncertainty in that fluence value was higher. On the other hand, obviously the physical chip that was tested was different as well. In any case, they can still be

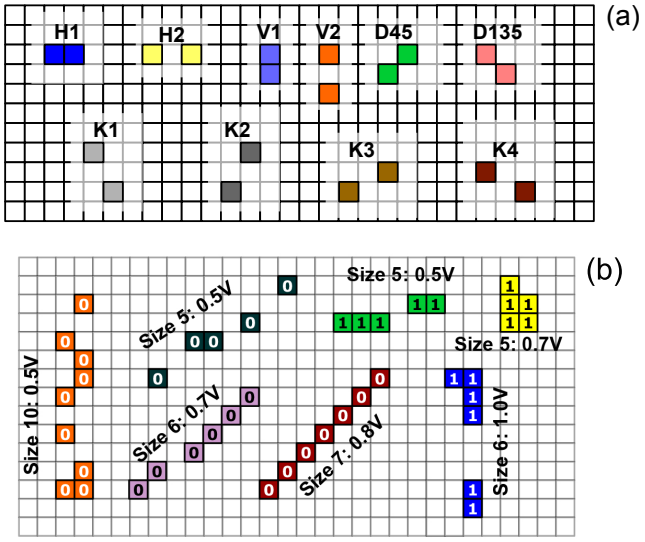

Figure 3. Shapes of the observed MCUs. (a) 2-bit MCUs. There are two types of horizontal ones (H1 and H2), two vertical ones (V1 and V2), two diagonal ones (D45 and D135), and 4 types of events disposed in chess-like knight-jump move (K1, K2, K3 and K4). (b) 5-bit to 10-bit MCUs. Values stored in the cell before the bitflip are shown.

considered acceptable since they are very similar. For 4-bit to 10-bit MCUs (not shown in the figure), error margins in the experimental cross sections are so high that it is impossible to reach any sound conclusions. Maybe the main point of disagreements between predictions and experimental results is the fact that MUSCA-SEP^3 did not predict events with multiplicity greater than 5, but experimentally, MCUs with larger multiplicities were observed. Thus, 2 6-bit MCUs were observed at 0.7V and 1.0V, respectively; a 7-bit MCU was observed at 1.0V; and a 10-bit MCU was observed at 0.5V (Table II). This is due to the fact that MUSCA-SEP^3 does not use exact data about the topology and internal organization of the memory cells, because this is proprietary information of the manufacturer. Approximations must be used instead and, as a consequence, the provided absolute values might disagree. However, the changes observed in the sensitivity of the memory at different voltages match quite accurately the experimental values (Figure 2). Hence, we can postulate MUSCA-SEP^3 as a good tool to make SRAM cross-section predictions at low bias voltages.

In these experiments, no microlatchups were observed. However, other authors, such as Hands et al. in 2012 [18] did report events with multiplicity up to 150 (which they attributed to microlatchups) in very similar 90-nm Cypress SRAMs. In that case, two samples of Cypress CY62148ELL and CY62148EV30LL were irradiated with fusion-produced neutrons at 14 MeV, at the ASP facility at the Atomic Weapons Establishment (AWE), Berkshire, U.K. [19]. In that case, the tested samples belonged to a different batch as the one that was tested in this paper, which clearly indicates that the manufacturer solved this problem in the release of further batches of the CY62148EV30LL SRAM. In addition, Samaras et al. [20] also reported a very high susceptibility of the CY62148EV30LL45ZSXI and CY62167EV30LL45ZXA 90-nm Cypress SRAMs to suffer microlatchups when exposed to heavy ions at nominal bias voltage. Although the work in this paper does not target radiation effects caused by heavy ions, in the future it would be interesting to carry out similar tests at ultra-low bias voltage, too.

Table IV
OCCURRENCE DISTRIBUTION OF THE MOST OFTEN 2-BIT MCUS: H1, V1, D45 AND D135

Round	H1	V1	D45	D135	Others
A (0.50V)	60.42%	10.42%	7.29%	9.38%	12.49%
B (0.60V)	65.17%	19.10%	4.49%	3.37%	7.87%
C (0.70V)	66.67%	22.92%	3.13%	2.08%	5.2%
D (0.80V)	62.89%	23.71%	4.12%	4.12%	5.16%
E (0.90V)	74.75%	14.14%	2.02%	3.03%	7.06%
F (1.00V)	75.32%	14.29%	2.60%	3.90%	3.89%
G (1.20V)	79.71%	7.25%	0%	7.25%	5.79%

By checking the sensitivity trends in Figure 2, it can also be observed that the SBU sensitivity significantly increases at very low voltages, especially at near-threshold ones, contrarily to that of MCUs. This trend is consistent with the results presented by Pawlowski et al. [21], where it can observed that the sensitivity for all types of MCUs barely increased in the range of 0.3V-1.0V.

The shape of the observed MCUs has also been analyzed. These results are presented in Figure 3, which is a physical representation of the SRAM bitcell topology. The memory that was examined implements bit interleaving, and we obtained the physical location of the observed bitflips by using proprietary unscrambling information from the manufacturer. The 2-bit MCUs were firstly studied in greater detail, since they were numerous enough to extract some conclusions. The types of the observed 2-bit MCUs are described in Figure 3a.

The percentages of observed events of each type are described in Table IV. In all the cases, the most often 2-bit MCU was H1, followed by V1. Diagonal ones were also representative, whereas other types of horizontal and vertical ones, as well as the knight-jump ones occurred very few times. In addition it seems that, as the bias voltage decreases, the H1 type of event is less likely to occur. We believe that this is due to any technological and proprietary parameters of the memory to which, as users, we do not have access.

The shapes of large MCUs were also studied (Figure 3b). It can be observed that they were linear or almost linear (following a horizontal, vertical or diagonal distribution). This is clearly due to a ionizing particle displaced as a consequence of the interaction with the impinging neutron, which flips cells along its track until it loses all its energy. If microlatchups had occurred, a complete block of information would have been affected completely, and this is not the case. This figure also shows the bit values of the affected cells before the bitflips occurred. There are distributed roughly 50%-50%, hence there is no dependency in the value (0 or 1). However, an additional interesting fact can be observed: all the bit values belonging to the same MCU are the same. Since the experiments were

carried out with the checkerboard pattern (0x55), this means that all the affected cells were placed in the same logical column. The reason being, in our opinion, that the power lines of the memory cells are distributed vertically.

IV. SER Predictions Issued by the MUSCA-SEP^3 Modeling Tool

This section discusses the impact of ultra low bias voltage for the 90-nm SRAM for an atmospheric environment. Results are based on MUSCA-SEP^3 predictions thanks to 90-nm SRAM sensitivity model deduced from experiments analysed in Section III. Two radiation fields have been discussed: ground and avionic, which have been issued from the modeling tools ATMORAD (*ATMOspheric RADiation*) [22].

A. Cross section calculation based on MUSCA-SEP^3

MUSCA-SEP^3 is a soft error prediction platform based on a Monte-Carlo approach that allows obtaining a complete simulation, ranging from the interaction of radiation particles with the matter to the occurrence of a SEE in the integrated circuit. The principle of the modeling is discussed in previous works [13], [23].

To model the 90 nm SRAM (planar bulk technology) devices, it is necessary to describe the active zones (drains and sources) and the Shallow-Trench Isolation (STI) topology. The methodology includes a General Design Specification (GDS) extractor, which allows deducing these details from GDSII files. Concerning the 90 nm SRAM studied in this paper, a reverse analysis was performed to deduce the elementary cell topology and the organization between adjacent cells (MCU investigation). The results of this analysis were presented in a previous work [24].

Concerning interactions, GEANT4 was used to develop and to integrate databases containing electron-hole pair densities induced by nuclear and ionization physical processes. Electron-hole pair's depositions occurring close to the sensitive areas were modeled from the 3D morphology database as a function of the ion energy, type and incidence angle [25].

Transport and collection mechanisms in the active area are crucial to evaluate the impact at semiconductor level (charge or transient). Indeed, 3D carrier morphology evolves according to mechanisms as well as drift (electric field), diffusion (carrier concentration gradient), collection and recombination processes. Bipolar amplifications can also be considered. Analytical models describing the transport and collection mechanisms were mainly issued from Technology Computer Aided Design (TCAD) simulations, and calibrated for investigated technological nodes.

Thus, MUSCA-SEP^3 aims at calculating SEE cross sections, including neutron, proton, muon, alpha and heavy ion contributions. It is important to note that nuclear and coulomb processes were simultaneously considered, which is crucial for protons. Conventional methods to calculate the cross section consist in calculating the ratio between the number of events and the particles fluence. Therefore, a more realistic approach consists in defining the probability of obtaining a given number of SEEs during a given time and for a given flux level [26].

B. Methodology to calculate the atmospheric SER

The sensitivity against SEEs of advanced nano-scale electronic devices is expected to increase, and recent studies have demonstrated the occurrence of SEEs due to cosmic-ray showers, which are composed by neutrons, protons and muons [27]–[30]. The type of secondary radiations and their intensity depend on the altitude, the geomagnetic latitude and the Sun's activity. For example, at sea level, muons are the most numerous terrestrial species. Thus, it is necessary to take into account the neutron, proton, and muon spectrum in order to assess the SER, particularly for ultra low bias voltage conditions, for which the critical charge is very low.

In order to study the effects of SEEs, it is also necessary to take into account the emitter alpha problematic induced by the contamination of the materials (wafer, package and radioactive specific materials in passivation and metallization layers).

The methodology that allows calculating the atmospheric SER is based on Equation 1.

$$SER = \sum_{p=n,p,\mu} \int \sigma_{SEE}(E,p) \cdot \frac{d\Phi_p(E,p)}{dE} \cdot dE + SER_\alpha \quad (1)$$

where $\frac{d\Phi_p(E,p)}{dE}$, $\sigma_{SEE}(E,p)$ and SER_α stand for the differential spectrum, the SEE cross section and the Alpha SER, respectively. The p index designates the particle type; i.e., neutron, proton or muon. SEE cross sections were calculated thanks to MUSCA-SEP^3. In this work, the atmospheric radiation fields (ground and avionic) were deduced by means of an atmospheric radiation model named ATMORAD [22], which is based on GEANT4 simulations of extensive Air Showers according to primary spectra which only depend on the solar modulation potential (Force-Field Approximation [31], [32]). Moreover, the solar potential is deduced from measurements issued from the neutron spectrometer operated by ONERA [33], [34] in the Pic-du-Midi (France, +2880 m above sea level) and the Concordia scientific station (Antarctica). The ground environment has been characterized by the geomagnetic location and altitude of the city of Toulouse (France, 141 meters above sea level), whereas a Paris - Los Angeles flight has been considered to investigate the avionic conditions.

Concerning Alpha radiation impurities, they can be found in some packaging materials and chemicals used in the fabrication process of the chip. The emission can range widely depending on the quantity and purification grade of the materials. MUSCA-SEP^3 can be adapted to investigate and quantify the α-SER contribution. However, the material properties required to define the α-emissivity types and their locations are rarely available. The alpha emitter contamination effect is considered as the sum of the package and wafer contributions (Equation 2).

$$SER_\alpha = SER_\alpha^{wafer} + SER_\alpha^{package} \quad (2)$$

where: $SER_\alpha^{wafer} = \sigma_\alpha^{wafer} \cdot \varepsilon_{wafer}$
and: $SER_\alpha^{package} = \sigma_\alpha^{package} \cdot \varepsilon_{package}$

ε_{wafer} and $\varepsilon_{package}$ are the wafer and package α-emissivities, respectively; and σ_α^{wafer} and $\sigma_\alpha^{package}$, the SEU cross sections.

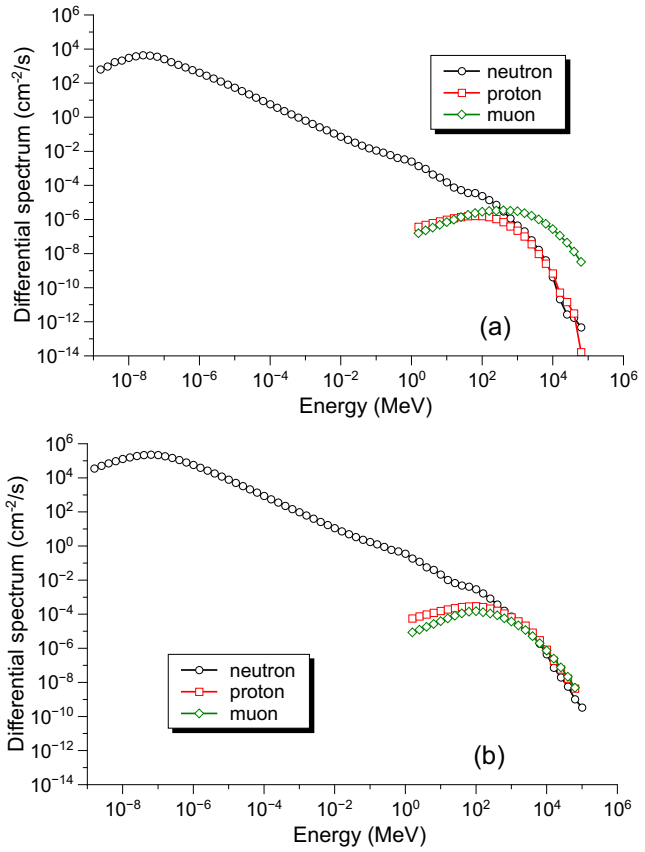

Figure 4. Characterization of the neutrons, protons and muons spectrum for (a) ground and (b) avionic radiation fields

In this first approach, we have considered a constant value for ε_{wafer} of 5×10^{-4} $\alpha \cdot cm^{-2} \cdot hr^{-1}$. This value was selected because it is typically considered for wafer emissivity [35]–[37] and because it corresponds to a Hyper-Low-Alpha (H.L.A. [38]) grade for package contamination. In fact, four alpha emission categories can be considered for $\varepsilon_{package}$:

- Hyper-Low-Alpha (H.L.A., $\varepsilon_{package} < 5{\times}10^{-4}$ $\alpha{\cdot}cm^{-2}{\cdot}$ hr^{-1}).
- Ultra-Low-Alpha (U.L.A., $\varepsilon_{package} < 10^{-3}$ $\alpha \cdot cm^{-2} \cdot$ hr^{-1}).
- Low-Alpha (L.A., $\varepsilon_{package} < 10^{-2}$ $\alpha \cdot cm^{-2} \cdot hr^{-1}$).
- Standard (S., $\varepsilon_{package} \sim 0.01 - 10$ $\alpha \cdot cm^{-2} \cdot hr^{-1}$).

In order to simplify the calculations, the alpha energy is considered equal to 6.5 MeV. This approach constitutes a very first step for determining the order of magnitude to be compared with the other contributions of concern (neutrons, protons and muons).

C. SER experimental results

Figure 4 presents the ground and avionic radiation fields including the neutrons, protons and muons spectrum. Although it was mentioned that a Paris - Los Angeles flight was considered to study the avionic conditions, Figure 4b shows the spectrum of the instantaneous geomagnetic position: Latitude = 61.35°, Longitude = -64.18° and Altitude = 11.58 km. Nevertheless,

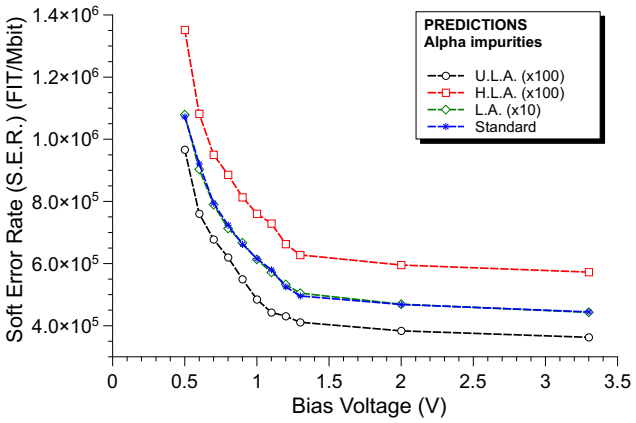

Figure 5. Calculated SER vs. bias voltage due to alpha emission categories (U.L.A., H.L.A., L.A. and Standard)

SER calculations discussed in Subsection IV-C2 consider the total flight.

1) SER for Ground radiation field: SER predictions at ground level were firstly carried out with MUSCA-SEP^3. Figure 5 shows the calculated SER due to α particles, which was obtained considering U.L.A., H.L.A., L.A. and Standard emission categories. Note that, for the sake of clarity, the curves for H.L.A. and U.L.A. have been multiplied by 100, and that of L.A. has been multiplied by 10. Besides, the SERs attributed to neutrons, protons and muons are presented in Figure 6 as a function of the bias voltage. In Figure 6a, different types of events multiplicity are categorized, from SBU to 6-bit. In this case, the curves for 4-bit, 5-bit and 6-bit have also been multiplied by 10. Both results allow evaluating the global SER for ground environment. As both figures show, the voltage decrease induces an increase in the SEU susceptibility against radiation, especially below 1.3V. For this technology, α-SER is the main contribution if the emission category is L.A. (Figure 5). Besides, the orders of magnitude issued from calculations are consistent with underground experiments [22], [39].

It is also interesting to investigate the separate neutrons, protons, and muons contributions to the SER, particularly at ultra low bias voltages. Thus, for the SER corresponding to SBUs in Figure 6a, these separate contributions have been calculated and presented in Figure 6b. The results suggest that muon-induced upsets start affecting the SER when the SRAM memory operates at bias voltages below 1.2V.

2) SER for Avionic radiation field: This subsection presents a similar analysis, but applied to the avionic environment (in particular, for heights at which commercial flights operate, ∼12 km). The results are presented in Figure 7. Figure 7a shows the SER vs. bias voltage, categorizing the events by multiplicity (from SBUs to 6-bit MCUs). As in the ground environment results, the SER increases as the bias voltage decreases, and it skyrockets when the SRAM is powered up at 1.2V or below. The contributions of neutron, proton and muon are presented in Figure 7b, and demonstrate that the main contribution is due to neutrons, regardless of the bias voltage. The contribution of muons start to become significant

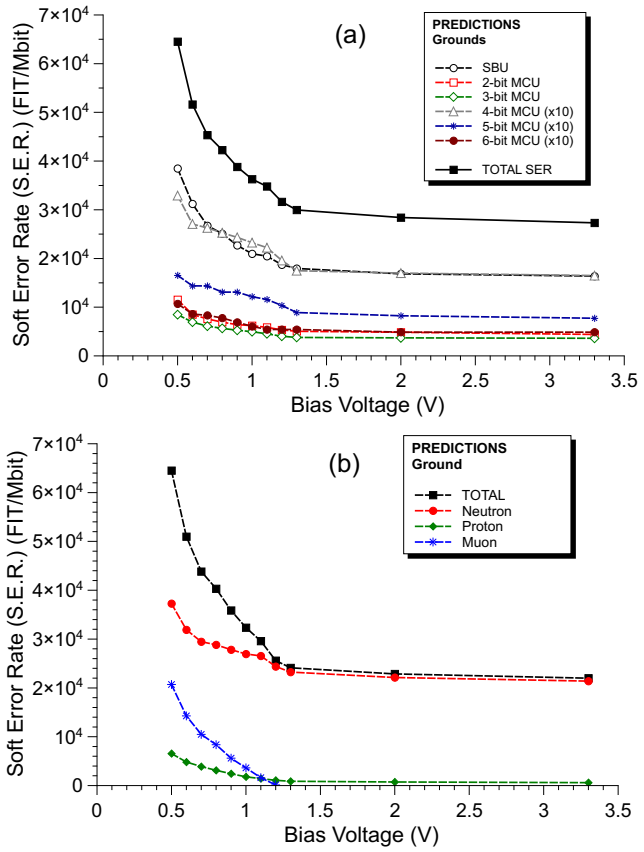

Figure 6. Calculated SER vs. bias voltage at ground level. (a) SBU to 6-bit MCU SER. (b) SER distinguishing the contributions of protons, neutrons and muons

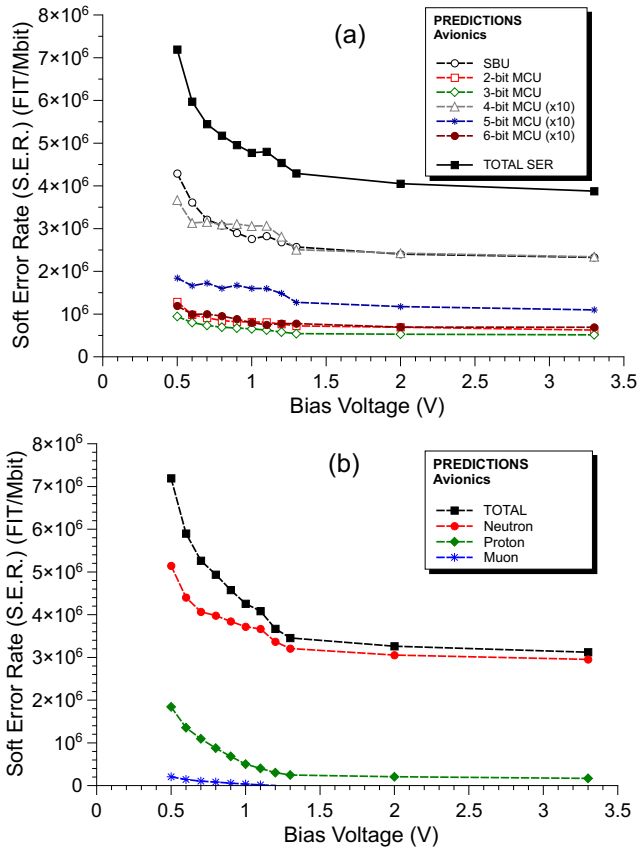

Figure 7. Calculated SER vs. bias voltage at the avionic level. (a) SBU to 6-bit MCU SER. (b) SER distinguishing the contributions of protons, neutrons and muons

below 1.2V, but it is still lower than that of the protons in all of the cases (note that Figure 6b shows the opposite for ground level, as expected). It would be interesting to conduct a similar analysis on more integrated technologies, mainly to investigate the contribution of direct ionization of protons.

Another interesting analysis that has been performed consisted in evaluating the total number of SEUs observed during commercial flights. Figure 8 presents predictions issued by MUSCA-SEP^3 for SEUs; in particular, for a Paris - Los Angeles flight, and distinguishing the contributions of SBUs and MCUs separately. These predictions have also been cross-checked with actual results. In 2009, an experimental platform developed by the authors including 1 Gigabit memory built with 64 16-Mbit 90-nm Cypress CY62167EV30LL-45ZXI SRAMs was used for SEU detection during said flights [40]. These memories belonged to a different batch than the ones tested at low voltage (Table I). Among them, it is remarkable to mention a Paris - Los Angeles flight, during which 15 bitflips were detected (6 SBUs, 1 double MBU, 2 double MCUs and 1 triple MCU). These data (6 bitflips due to SBUs and 9 bitflips due to MBUs/MCUs) were in good agreement with the estimations. They are also displayed in Figure 8. In that case, the SRAMs were powered up at nominal bias voltage.

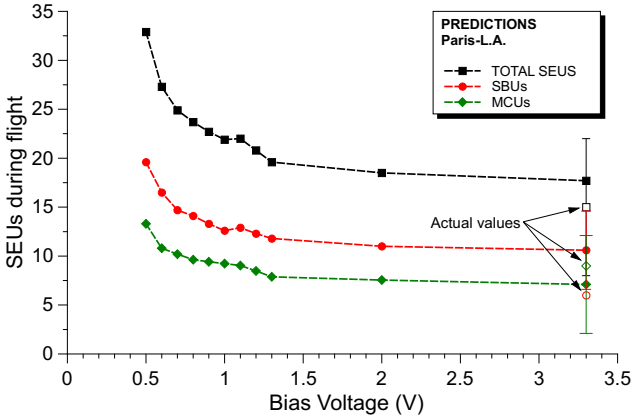

Figure 8. Calculated SEU, SBU and MCU number as a function of bias voltage for a Paris - Los Angeles flight

V. Conclusions

This paper has presented the sensitivity characterization of the COTS CMOS 16-Mbit SRAM CY62167EV30LL-45ZXI manufactured by Cypress Semiconductor, when powered up at ultra-low bias voltage. Firstly, experimental results carried out with 14-MeV neutrons at GENEPI2 facility have shown a clear evidence of the increase in the neutron cross section at ultra-low bias voltages, especially below 1.3V. These results were mostly in concordance with theoretical cross-section

predictions issued by the modeling tool MUSCA-SEP^3. However, discrepancies on MCUs at lower voltages were found, which have been attributed to the statistical error made in the predictions with few data. Finally, MUSCA-SEP^3 also issued SER predictions that allowed characterizing the sensitivity of this memory at different radiation fields (ground and avionics); for neutrons, protons, muons and α particles.

REFERENCES

[1] J. A. Abraham, E. S. Davidson, and J. H. Patel, "Memory System Design for Tolerating Single Event Upsets," *IEEE Tran. Nucl. Sci.*, vol. 30, pp. 4339–4344, Dec. 1983.

[2] J. A. Maestro and P. Reviriego, "Reliability of Single-Error Correction Protected Memories," *IEEE Tran. Reliab.*, vol. 58, pp. 193–201, Mar. 2009.

[3] R. Velazco and F. J. Franco, "Single Event Effects on Digital Integrated Circuits: Origins and Mitigation Techniques," in *IEEE International Symposium on Industrial Electronics*, pp. 3322–3327, Jun. 2007.

[4] R. C. Baumann, "Radiation-Induced Soft Errors in Advanced Semiconductor Technologies," *IEEE Tran. Dev. Mat. Reliab.*, vol. 5, pp. 305–316, Sep. 2005.

[5] M. P. King *et al.*, "Electron-Induced Single-Event Upsets in Static Random Access Memory," *IEEE Tran. Nucl. Sci.*, vol. 60, pp. 4122–4129, Dec. 2013.

[6] A. Kumar, J. Rabaey, and K. Ramchandran, "SRAM supply voltage scaling: A reliability perspective," in *10th International Symposium on Quality Electronic Design*, pp. 782–787, Mar. 2009.

[7] M. M. H. Galib, I. J. Chang, and J. Kim, "Supply Voltage Decision Methodology to Minimize SRAM Standby Power Under Radiation Environment," *IEEE Tran. Nucl. Sci.*, vol. 62, pp. 1349–1356, Jun. 2015.

[8] P. Hazucha *et al.*, "Neutron Soft Error Rate Measurements in a 90-nm CMOS Process and Scaling Trends in SRAM from 0.25-/spl mu/m to 90-nm Generation," in *IEEE International Electron Devices Meeting (IEDM)*, pp. 21.5.1–21.5.4, Dec. 2003. Available at: http://doi10.1109/IEDM.2003.1269336.

[9] H. Fuketa, M. Hashimoto, Y. Mitsuyama, and T. Onoye, "Neutron-Induced Soft Errors and Multiple Cell Upsets in 65-nm 10T Subthreshold SRAM," *IEEE Tran. Nucl. Sci.*, vol. 58, pp. 2097–2102, Aug. 2011.

[10] J. A. Clemente *et al.*, "Single Events in a COTS Soft-Error Free SRAM at Low Bias Voltage Induced by 15 MeV Neutrons," *IEEE Tran. Nucl. Sci.*, vol. 63, pp. 2072–2079, Aug. 2016.

[11] F. Villa, M. Baylac, S. Rey, O. Rossetto, W. Mansour, P. Ramos, R. Velazco, and G. Hubert, "Accelerator-Based Neutron Irradiation of Integrated Circuits at GENEPI2 (France)," in *IEEE Radiation Effects Data Workshop (REDW)*, pp. 1–5, July 2014. Available at: http://dx.doi.org/10. 1109/REDW.2014.7004511.

[12] F. Villa *et al.*, "Multipurpose applications of the accelerator-based neutron source[1pt] GENEPI2," *Nuovo Cimento C Geophysics Space Physics C*, vol. 38, p. 182, Nov. 2016. Available at: http://adsabs.harvard.edu/abs/2016NCimC..38..182V.

[13] G. Hubert, S. Duzellier, C. Inguimbert, C. Boatella-Polo, F. Bezerra, and R. Ecoffet, "Operational SER Calculations on the SAC-C Orbit Using the Multi-Scales Single Event Phenomena Predictive Platform (MUSCA-SEP3)," *IEEE Tran. Nucl. Sci.*, vol. 56, pp. 3032–3042, Dec. 2009.

[14] J. A. Clemente, G. Hubert, F. J. Franco, F. Villa, M. Baylac, H. Mecha, and R. Velazco, "Evaluation of the Sensitivity of a COTS 90-nm SRAM Memory at Low Bias Voltage," in *16th European Conference on Radiation Effects on Components and Systems (RADECS)*, Sep. 2016.

[15] J. A. Clemente *et al.*, "Statistical Anomalies of Bitflips in SRAMs to Discriminate SBUs From MCUs," *IEEE Tran. Nucl. Sci.*, vol. 63, pp. 2087–2094, Aug. 2016.

[16] R. Velazco *et al.*, "Evidence of the Robustness of a COTS Soft-Error Free SRAM to Neutron Radiation," *IEEE Tran. Nucl. Sci.*, vol. 61, pp. 3103–3108, Dec. 2014.

[17] International Technology Roadmap for Semiconductors (ITRS), "http://www.itrs2.net/," 2016.

[18] A. Hands, P. Morris, K. Ryden, and C. Dyer, "Large-Scale Multiple Cell Upsets in 90 nm Commercial SRAMs During Neutron Irradiation," *IEEE Tran. Nucl. Sci.*, vol. 59, pp. 2824–2830, Dec. 2012.

[19] AWE Radiation Sciende homepage [Online]., "http://www.awe.co.uk/what-we-do/science-engineering-technology/radiation-science/," 2016.

[20] A. Samaras, "Single Event Upset cross section dose dependence on 90nm SRAM, ESA/ESTEC," 2013. Available at https://escies.org/download/webDocumentFile?id=60351.

[21] R. Pawlowski *et al.*, "Characterization of Radiation-Induced SRAM and Logic Soft Errors from 0.33V to 1.0V in 65nm CMOS," in *IEEE Proceedings of the Custom Integrated Circuits Conference (CICC)*, Sep. 2014. Available at: http://dx.doi.org/10.1109/CICC.2014.6946138.

[22] G. Hubert and A. Cheminet, "Radiation Effects Investigations Based on Atmospheric Radiation Model (ATMORAD) Considering GEANT4 Simulations of Extensive Air Showers and Solar Modulation Potential," *Radiat. Res.*, vol. 184, pp. 83–94, July 2015.

[23] L. Artola *et al.*, "SEU Prediction From SET Modeling Using Multi-Node Collection in Bulk Transistors and SRAMs Down to the 65 nm Technology Node," *IEEE Tran. Nucl. Sci.*, vol. 58, pp. 1338–1346, Jun. 2011.

[24] L. Artola *et al.*, "In Flight SEU/MCU Sensitivity of Commercial Nanometric SRAMs: Operational Estimations," *IEEE Tran. Nucl. Sci.*, vol. 58, pp. 2644–2651, Dec. 2011.

[25] M. Raine *et al.*, "Impact of the Radial Ionization Profile on SEE Prediction for SOI Transistors and SRAMs Beyond the 32-nm Technological Node," *IEEE Tran. Nucl. Sci.*, vol. 58, pp. 840–847, Jun. 2011.

[26] G. Hubert and R. Ecoffet, "Operational Impact of Statistical Properties of Single Event Phenomena for On-Orbit Measurements and Predictions Improvement," *IEEE Tran. Nucl. Sci.*, vol. 60, pp. 3915–3923, Oct. 2013.

[27] B. D. Sierawski *et al.*, "Impact of Low-Energy Proton Induced Upsets on Test Methods and Rate Predictions," *IEEE Tran. Nucl. Sci.*, vol. 56, pp. 3085–3092, Dec. 2009.

[28] B. D. Sierawski *et al.*, "Muon-Induced Single Event Upsets in Deep-Submicron Technology," *IEEE Tran. Nucl. Sci.*, vol. 57, pp. 3273–3278, Dec. 2010.

[29] G. Hubert, L. Artola, and D. Regis, "Impact of scaling on the soft error sensitivity of bulk, FDSOI and FinFET technologies due to atmospheric radiation," *Integration, the VLSI Journal*, vol. 50, pp. 39–47, 2015.

[30] G. Hubert, P. L. Cavoli, C. Federico, L. Artola, and J. Busto, "Effect of the Radial Ionization Profile of Proton on SEU Sensitivity of Nanoscale SRAMs," *IEEE Tran. Nucl. Sci.*, vol. 62, pp. 2837–2845, Dec. 2015.

[31] L. J. Gleeson and W. I. Axford, "Solar Modulation of Galactic Cosmic Rays," *Astrophy. J.*, vol. 154, p. 1011, 1968. Available at: http://dx.doi.org/10.1086/149822.

[32] A. Cheminet, G. Hubert, V. Lacoste, D. Maurin, and L. Derome, "Cosmic Ray Solar Modulation and Forbush Decrease Analyses Based on Atmospheric Neutron Spectrometry at Mountain Altitude and GEANT4 Simulations of Extensive Air Showers," *J. Geophys. Res.- Space*, vol. 118, no. 12, pp. 7488–7496, 2013.

[33] G. Hubert, C. Federico, M. Pazianotto, and O. Gonzales, "Long and short-term atmospheric radiation analyses based on coupled measurements at high altitude remote stations and extensive air shower modeling," *Astropart. Phys.*, vol. 74, no. 1, pp. 27–36, 2016.

[34] G. Hubert, "Analyses of cosmic ray induced-neutron based on spectrometers operated simultaneously at mid-latitude and antarctica high-altitude stations during quiet solar activity," *Astropart. Phys.*, vol. 83, pp. 30–39, 2016.

[35] R. Heald, "How Cosmic Rays Cause Computer Downtime," *IEEE Rel. Soc. SCV Meeting*, 2005. Available at http://www.ewh.ieee.org/r6/scv/rl/articles/ser-050323-talk-ref.pdf.

[36] J. F. Ziegler and H. Puchner, "SER-History, Trends and Challenges," *Cypress Semiconductors*, 2004.

[37] R. Baumann and E. Smith, "Call for improved ultra-low background alpha-particle emission metrology for the semiconductor industry," *Int. SEMATECH Technology Transfer*, vol. #01054118A-XFR, 2001. Available at http://www.sematech.org/docubase/document/4118axfr.pdf.

[38] X. Zhu, "Logic SER characterization, Tutorial," *2008 International Reliability Physics Symposium (IRPS)*, 2008.

[39] A. Lesea, K. Castellani-Coulie, G. Waysand, J. L. Mauff, and C. Sudre, "Qualification Methodology for Sub-Micron ICs at the Low Noise Underground Laboratory of Rustrel," *IEEE Tran. Nucl. Sci.*, vol. 55, pp. 2148–2153, Aug. 2008.

[40] P. Peronnard, R. Velazco, and G. Hubert, "Real-Life SEU Experiments on 90 nm SRAMs in Atmospheric Environment: Measures Versus Predictions Done by Means of MUSCA SEP3 Platform," *IEEE Tran. Nucl. Sci.*, vol. 56, pp. 3450–3455, Dec. 2009.